Attorney's Docket No. 5649-952 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Jae-goo Lee
Serial No.: 10/068,148 Group Art Unit: 2818
Filed: February 6, 2002 Examiner: To Be Assigned
For: INTEGRATED CIRCUIT MEMORY DEVICES PROVIDING PER-BIT REDUNDANCY AND METHODS OF OPERATING SAME

Date: December 3, 2002

Commissioner for Patents
Washington, DC 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

The documents listed on the attached PTO-1449 were cited in a Notice of Office Action of corresponding Korean Application No. 10-2001-0007276. Each document listed on the attached PTO-1449 was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement. A copy of each document, including the Notice of Office Action, is enclosed. The Commissioner is hereby authorized to charge any additional fee, which may be required, or credit any refund, to our Deposit Account No. 50-0220.

These items are cited herein because they were cited in the Notice of Office Action of the corresponding Korean application. The Examiner may also wish to consider the notations on the Search Report itself regarding the relevance of each item.

It is requested that these references be considered by the Examiner and officially made of record in accordance with the provisions of 37 CFR 1.97 and Section 609 of the MPEP.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, on December 3, 2002

Candi L. Riggs; Date of Signature: December 3, 2002